Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

No amendments have been made to the claims.

Listing of the Claims:

1. (Original) A method comprising:

forming a logic gate stack in a logic region on a substrate;

forming a flash memory gate stack in a flash region on the substrate;

depositing a hardmask layer over the logic gate stack and over the flash memory gate stack;

patterning the hardmask in the logic region so that areas of hardmask remain where logic gates are desired;

patterning the flash gate stack in the flash region to form flash memory gates; and

etching the logic gate stack using the remaining hardmask as a mask to form logic gates.

2. (Original) The method of claim 1, wherein the logic region and the flash region are located on a single die.

3. (Original) The method of claim 2, wherein the logic gate stack is comprised of a gate dielectric layer and a gate electrode layer.

4. (Original) The method of claim 2, wherein the flash memory gate stack is comprised of a gate dielectric layer, a floating gate layer, an inter-electrode dielectric layer, and a control gate electrode layer.

5. (Original) The method of claim 1, further comprising removing the hardmask layer.

6. (Original) The method of claim 1, wherein the hardmask layer consists of an anti-reflective coating (ARC) hardmask layer.

7. (Original) The method of claim 6, wherein the ARC hardmask layer is comprised of one or more materials selected from the group consisting of oxide, oxynitride, nitride, and carbon.

8. (Original) The method of claim 6, wherein the ARC hardmask layer is sufficiently damaged by the final logic gate stack etch that it may be easily removed.

9. (Original) The method of claim 1, further comprising depositing a masking layer over the flash region after patterning the flash gate stack and before etching the logic gate stack to form logic gates.

10. (Original) The method of claim 1, wherein the flash memory gates have a length of less than 150 nm and have a pitch of less than 400 nm, and the logic gates have a length of less than 150 nm.

11. (Original) A method comprising:

forming a logic gate stack in a logic region on a substrate;

forming a flash memory gate stack in a flash region on the substrate;

depositing an anti-reflective coating (ARC) hardmask layer over the logic gate stack and over the flash memory gate stack;

depositing a first layer of resist over the logic region and the flash region;

patterning the first layer of resist in the logic region and etching the first layer of resist and the ARC hardmask layer in the logic region, leaving areas of the first layer of resist and hardmask over the areas where logic gates are desired;

removing the first layer of resist from the logic region and the flash region;

depositing a second layer of resist over the logic region and the flash region;

patterning the second layer of resist in the flash region and etching the second layer of resist, the ARC hardmask layer, and the flash memory gate stack in the flash region to form flash memory gates;

removing the second layer of resist from the logic region and the flash region;

depositing a third layer of resist over the flash region; and

etching the logic gate stack to form logic gates using the remaining ARC hardmask as a mask.

12. (Original) The method of claim 11, further comprising removing the third layer of resist from the flash region.

13. (Original) The method of claim 11, wherein the logic region and the flash region are located on a single die.

14. (Original) The method of claim 11, wherein the logic gate stack is comprised of a gate dielectric layer and a gate electrode layer.

15. (Original) The method of claim 11, wherein the flash memory gate stack is comprised of a gate dielectric layer, a floating gate layer, an inter-electrode dielectric layer, and a control gate electrode layer.

16. (Original) The method of claim 11, wherein the ARC hardmask layer is comprised of one or more materials selected from the group consisting of oxide, oxynitride, nitride, and carbon.

17. (Original) The method of claim 11, wherein the flash memory gates have a length of less than 150 nm and a pitch of less than 400 nm, and the logic gates have a length of less than 150 nm.

18. (Original) An apparatus comprising:

a substrate, the substrate having a logic region and a flash region;

a logic gate stack formed on the substrate in the logic region, the logic gate stack having a top surface;

regions of anti-reflective coating (ARC) formed on the top surface of the logic gate stack, the regions of ARC covering the areas of the logic gate stack where logic gates are to be formed;

a plurality of flash memory gates formed on the substrate, the flash memory gates having a top surface; and

a layer of resist, wherein the resist covers at least the top surface of the logic gate stack, the regions of ARC formed on top of the logic gate stack, and the top surface of the flash memory gates.

19. (Original) The apparatus of claim 18, wherein the logic gate stack is comprised of a gate dielectric layer and a gate electrode layer.

20. (Original) The apparatus of claim 18, wherein the flash memory gates are comprised of a gate dielectric layer, a floating gate layer, an inter-electrode dielectric layer, and a control gate electrode layer.

21. (Original) The apparatus of claim 18, wherein the ARC is comprised of one or more materials selected from the group consisting of oxide, oxynitride, nitride, and carbon.

22. (Original) The apparatus of claim 18, wherein the flash memory gates have a gate length of less than 150 nm and a pitch of less than 400 nm.

23. (Original) A method comprising:

forming a first stack in a first region on a substrate and a second stack in a second region on the substrate, wherein the second stack is thicker than the first stack;

depositing a hardmask layer over the first stack and the second stack;

patterning the first region to remove portions of hardmask in the first region;

patterning the second region to remove portions of the hardmask in the second region and portions of the second stack to form the desired geometries of the second stack; and

removing portions of the first stack using the remaining portions of hardmask as a mask to form the desired geometries of the first stack.

24. (Original) A method comprising:

forming a logic gate stack in a logic region on a substrate;

forming a flash memory gate stack in a flash region on the substrate;

depositing a hardmask layer over the logic gate stack and over the flash memory gate stack;

patterning the hardmask in the logic region so that areas of hardmask remain where logic gates are desired;

patterning the flash gate stack in the flash region and etching away the hardmask layer and a portion of the flash memory gate stack in the flash region to form a partial flash memory gate; and

etching the logic gate stack and the remainder of the flash memory gate stack using the remaining hardmask as a mask to form logic gates and flash memory gates.

25. (Original) The method of claim 24, wherein the logic region and the flash region are located on a single die.

26. (Original) The method of claim 24, wherein the hardmask layer comprises an anti-reflective coating (ARC) hardmask layer.

27. (Original) The method of claim 24, wherein the ARC hardmask layer is comprised of one or more materials selected from the group consisting of oxide, oxynitride, nitride, and carbon.

28. (Original) The method of claim 24, wherein the flash memory gates have a length of less than 150 nm and a pitch of less than 400, and the logic gates have a length of less than 150 nm.